Design Approaches for Hybrid CMOS/Molecular Memory based on Experimental Device Data

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ABSTRACT

In recent years many advances have been made in the development of molecular scale devices. Experimental data shows that these devices have potential for use in both memory and logic. This paper describes the challenges faced in building crossbar array based molecular memory, and develops a methodology to optimize molecular scale architectures based on experimental device data taken at room temperature. In particular, we discuss reading and writing such memory using CMOS and compiling a solution for easily reading device conductivity states (typically characterized by very small currents). Additionally, a metric is derived to determine the voltages for writing to the crossbar array. Simulation results, incorporating experimental device data, are presented using Cadence Spectre.

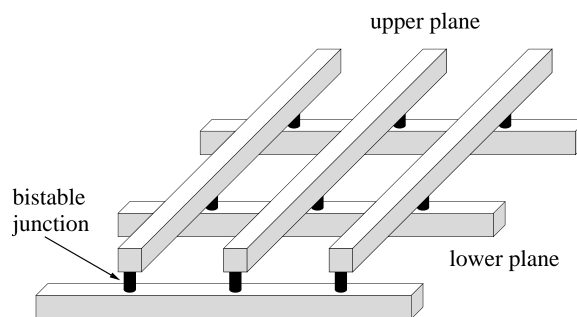

Figure 1: The crossbar paradigm consists of perpendicular sets of parallel wires with bistable junctions at each wire crossing.

1. INTRODUCTION

The infant field of molecular nanoelectronics is often defined as including any technology whose device feature sizes are on the scale of single molecules [5]. One intriguing technology family within this field consists of devices based on self-assembled monolayers (SAM) of molecules sandwiched between two conducting terminals. Experiments have shown how such devices could be fabricated with useful properties such as rectification, hysteresis and negative differential resistance [2, 3, 11, 14]. Researchers are also making great strides towards integrating these devices into novel electronic circuits [10]. As molecular electronics matures to the point of fabricating molecular memory and logic, circuit level considerations must be assessed in order to expedite development.

A common structure in which SAM-based devices have been considered and fabricated to date is known as the crossbar array, which consists of two sets of parallel wires crossing perpendicularly [18]. Between each wire crossing exists a SAM of molecules such that the overall circuit is an array of two-terminal molecular devices. If the devices are programmable, as are the ones considered in this paper, then the resulting circuit can be used to implement either memory or programmable logic. As can be seen in Fig. 1, a crossbar array is a regular structure which eases fabrication, a primary motivation for using such circuits. Some in the field, including H-P Labs and Caltech, have already accomplished the fabrication of molecular crossbar arrays for use as memory and are continuing toward the development of larger, denser arrays [1,10]. As such circuits scale to accommodate greater memory and logic requirements, circuit level issues, which may limit scaling, must be addressed.

The device explored here is a SAM-based molecular device that shows electrical switching with memory (hysteresis). Circuit simulations are used to evaluate the potential of this device for use as a building block for memory and programmable logic. The molecule this device is based on is commonly known as the "nitro" molecule and it exhibits this hysteric behavior, which is essential for the operation of crossbar array based memory circuits.

In this paper we examine some of the circuit level challenges to overcome in the development of crossbar array

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based circuits. In particular, we discuss reading and writing the crossbar array based memory from CMOS, compiling a solution for reading very small currents through these molecular devices, and a metric to calculate voltages for writing to the crossbar array. We discuss memory size limitations based on device rectification and on/off current ratios. Proposed is a design approach for minimizing the effects of these limitations that touches on both circuit and device level improvements. Using Cadence Spectre, we present room temperature simulation results for reading and writing the crossbar array. All models for our "nitro" molecule are developed using the universal device model (UDM) [16] developed at the University of Virginia. Likewise, simulations of hybrid CMOS/Nano circuits make use of the 45nm MOSFET predictive technology model (PTM) from the University of California, Berkeley.

2. MOLECULAR ELECTRONIC DEVICES AND CIRCUITS

2.1 Experimental Results: Electrical Behavior of a Molecular Device

In the area of molecular electronics, researchers are exploring different combinations of organic molecules with varying electrical behaviors and molecular structures. We have designed such a device structure and tested an oligo(phenylene ethynylene) molecule with a nitro sidegroup (Fig. 2a), a molecule that has shown potential for use in logic as well as memory. The test structure that we have designed and fabricated is shown in Fig. 2b and is called the nanowell device [12]. This device consists of a "well" with a diameter of 10-50 nm, a depth of 100nm, silicon dioxide sides, and a gold bottom.

The starting substrate for the nanowell is a silicon wafer covered with silicon dioxide, patterned with gold and a top layer of silicon dioxide 100nm thick. A focused ion beam (FIB) is used to mill the well through the top silicon dioxide to expose the bottom Au. This structure is then placed into a solution of the self-assembling molecules, each containing a sulfur endgroup giving it a chemical affinity for gold. These molecules assemble in an upright position on the gold surface, forming only a single monolayer of molecules. Once assembled, a top contact is made by evaporating titanium and then gold on the molecules in the device. This results in the completed nanowell device illustrated in Fig. 2b. The top and bottom contacts can be probed to measure currents through the devices.

Different groups have observed varying electrical characteristics from this molecule that include an asymmetric hysteretic behavior [3,4,6,8,9,15]. This behavior is again shown in the experimental room temperature I-V results of Fig. 3. One can observe in Scan 1 that at -2.3 V, the current switches from a high conductivity state to a low conductivity state and then continues on a lower conductivity path. We labeled -2.3 V in Fig. 3 as -V_{toggle} to signify that this is the switching point, or toggle voltage. In Scan 2, the voltage is again applied from 0 to -3 V and the current remains in the low conductivity state as expected. In Scan 3, we apply a voltage bias from 0 V to +3 V, and one can observe a change in the slope of the I-V curve around +2.5 V on the forward bias. This sudden increase in current marks the transition from the low conductivity state to the high conductivity state; we call this the forward bias toggle voltage (+V_{toggle}). Scan 4 shows that as the forward bias is applied from 0 V to +3 V again, the device remains in the high conductivity state.

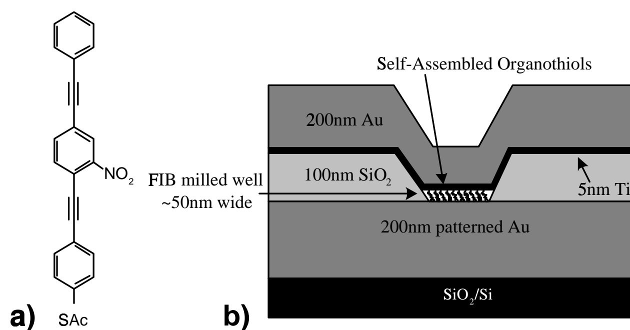

Figure 2: (a) The nitro-OPE molecule, which had its acetate moiety removed with acid during the assembly process of the free thiol. (b) A cross-section of the nanowell device.

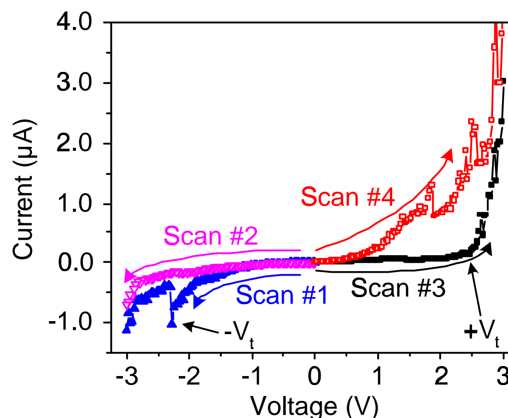

Figure 3: Room temperature I-V characteristics of nitro molecule monolayer showing switching with memory behavior.

2.2 Modeling the Molecular Device for Circuit Simulation

It is clear from inspection of Fig. 3 that this device exhibits a number of non-classical characterisitics. One obvious non-classical element is the hysteresis between the high and low conductivity states, however the device in general is very non-linear and is not easily represented by standard SPICE models. Thus, we have chosen to use the universal device dodel (UDM) [16] from the University of Virginia to model the characteristics of our "nitro" device. In general, the UDM models the I-V characteristics of such devices from a set of four possible equations representative of behavior common to nanoscale devices: linear (resistor-like) behavior, thermionic emission (diode equation), resonant tunneling (Gaussian equation) and coulomb blockade (step function). The UDM is capable of accepting experimental data for devices such as that shown in Fig. 3, and using it to create a Verilog-A model file, consisting of these four types of equations, for our device. This model is then utilized by

Cadence Spectre during circuit simulations.

2.3 The Crossbar Array Including Applications

As stated previously, the crossbar array is a plane of parallel nanowires crossing another plane of parallel nanowires perpendicularly, with a SAM of molecules sandwiched in between each wire crossing. In general, crossbar-based architectures have several nice features such as programmability, low-cost fabrication and high device densities. Specifically, the regularity of the crossbar structure necessitates only one mask for fabrication. This mask can be used for both sets of nanowires, which greatly reduces fabrication costs.

In this paper, we will study the crossbar array used as molecular memory. As technology advances, memory device density inherently gets larger. The crossbar array gives the ultimate advantage in density, storing one bit at every single wire junction in the crossbar. In order to utilize these crossbar arrays as memory structures, we need to create an efficient way to read and write these memory cells. In our 50nm $\times$ 50nm "nitro" device, the measured currents are typically in the single μA range, giving our devices inherent resistances around 1MΩ. As devices are scaled smaller, these output currents also become smaller, making it hard to determine what exactly is stored in the molecular devices. In fact, it is not uncommon to see device currents on the order of 100pA [2, 14].

In the following sections we discuss methods to optimize the reading and writing process, aiming to assuage limitations posed by inherent device and circuit level characteristics. Since the crossbar array, by itself, is not capable of signal restoration or inversion, some type of CMOS architecture is necessary to perform the read and write functions. Discussed are ways to read and write from CMOS, and ways to optimally augment the crossbar array with CMOS circuitry.

3. CHALLENGES IN DEVELOPING MOLECULAR MEMORY

Using molecular switches for memory seems natural since they are essentially tunable devices that can be set into one of two possible conductivity states, one representing logic '1' and the other logic '0'. A device can be written by applying a large magnitude voltage across it where exceeding a positive threshold will force the device into the logic '1' state and a large negative threshold will write a logic '0'. Reading can be achieved simply by applying a voltage smaller than the thresholds and measuring the output current (I_{out}). It is for this reason that an important metric of analysis for such a memory circuit is the ratio of the output currents for logic '1' and logic '0', referred to here as the '1'/'0' current ratio ($F_{1/0} = I_{out1}/I_{out0}$).

3.1 Effects of Large Reverse Bias Currents

To effectively read data from nanoscale memory, the output '1'/'0' current ratio ($F_{1/0}$) must be as large as possible and must always be greater than one. When this ratio is too small difficulty arises in trying to distinguish a logic '1' from a logic '0'. Since it is desirable that $F_{1/0}$ be as large as possible, the exploration of any device and circuit level factors affecting this ratio becomes an important endeavor.

One device level characteristic directly affecting $F_{1/0}$ is the ratio between the forward and reverse bias currents ($F_{f/r}$) or rectification ratio. The closer $F_{f/r}$ is to one, the closer the device behavior is to that of a resistor. Likewise, device behavior is like that of a diode for $F_{f/r} \gg 1$. Thus, it is this ratio that determines the amount of current that flows through parts of the array that are not selected for reading. This can be understood by considering that as the device is more diode-like ($F_{f/r} \gg 1$), the undesirable nets in Fig. 5 that are parallel to the device being read are essentially cut-off due to the reverse bias of the diodes.

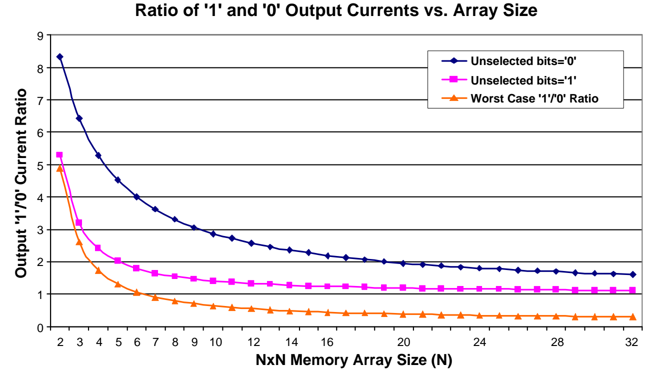

Figure 4: Maximum array size limited by On/Off ratio of molecular switches.

Looking at it another way, one could model the devices that are reverse biased with a higher resistance than those that are forward biased. By modeling the devices simply as resistors, a resistor network is obtained consisting of the device being read (R_{rd}) in parallel with an equivalent resistance for the unselected devices (R_{unsel}). If the ratio $F_{f/r}$ is close to one, the resistance R_{unsel} is closer to and may exceed R_{rd} of the selected bit. From this perspective, it can be seen that for a large sized array many devices in the unselected circuit path are in parallel such that R_{unsel} becomes small. In fact, there is a minimum array size at which $R_{rd} \approx R_{unsel}$ leading to a '1'/'0' ratio $F_{1/0} \approx 1$. For larger arrays where $R_{rd} < R_{unsel}$ the current representing logic '0' becomes greater than that representing logic '1'.

The point at which the output currents representing logic '1' and logic '0' become indistinguishible can be seen in Fig. 4. In this figure, the output ratio $F_{1/0}$ is plotted against the array size. These results are for the device described in section 2.1 where the ratio between on and off device currents is about 10. The first point to be noticed from this plot is that $F_{1/0}$ is smaller for larger sized arrays showing a limit on array size. Worth noting is that these results assume that all unselected rows and columns are left floating while a bias is applied only to the row and column of the selected device. If the unselected rows and columns are grounded this plot would show a larger maximum array size. It is also worth mentioning that for larger $F_{f/r}$, the ratio $F_{1/0}$ is improved for large arrays. Thus, one way to improve the maximum allowed size of a crossbar memory array is to increase the device property $F_{f/r}$.

3.2 Reading Nanoscale Memory from CMOS

Another important consideration for the design of integrated circuits based on molecular crossbar arrays is that the currents through many molecular devices fabricated to

date are much smaller than what is common for conventional bulk Si devices. More specifically, many molecular electronic devices have been fabricated which exhibit measured currents on the order of nanoamps or even hundreds of picoamps [2, 14]. In an IC composed of both molecular devices and CMOS circuitry the currents out of the nanoscale circuits may be too small to be accurately sensed using CMOS amplifiers. For the device described in section 2.1, operating currents are actually on the order of microamps, a feature that may make such devices advantageous for circuit development. However, considering that these devices have been fabricated in nanowells with dimensions of about 50nm × 50nm, it is important to note that currents through scaled versions of these molecular devices will be much smaller. It is thus important to consider circuit level design techniques for both nanoscale and CMOS circuitry that would allow more tractable methods of reading and writing the memory array.

4. DESIGN SOLUTIONS

4.1 Device Level Considerations

As mentioned in section 3.1, array size is limited by the device ratio between forward and reverse bias currents ($F_{f/r}$). Since a larger $F_{f/r}$ leads to larger maximum array sizes it is worthwhile to explore methods for increasing this ratio at the device level.

Kushmerick et al. [7] and Reed et al. [17] have provided evidence suggesting that it is possible to tune the rectification or current-voltage asymmetry either by changing the end group of the molecular device or by changing the actual metal contact [7]. In other words, the asymmetry observed in the molecular current-voltage characteristics may be caused by the differences in the metal-molecule coupling at the two contacts. Experiments were performed with a number of different molecular end groups, including the sulfur end group used here, each yielding different asymmetric results [7]. Asymmetry has additionally been observed from a symmetric molecule when using Au and Pd as contacts instead of using Au for both contacts [7]. This shows that the asymmetry in the contacts can cause asymmetric I-V characteristics regardless of the type of molecule. Theoretically, this Au-Pd contact combination should increase the device rectification ratio for an asymmetric molecular device, such as the nitro device, however more experimentation is needed to verify this.

4.2 Design Options for a CMOS Interface

In order to deal with the potential difficulty in reading a nanomemory using CMOS (as described in section 3.2 and Fig. 5) we propose the addition of at least one row of molecular devices that act as a load to the selected device. More specifically, devices in this extra row are connected to a source voltage on one end and share a column with devices in the memory on the other such that they are series connected. The signal to be read by CMOS is then a voltage at the node between the device being read and another in the row of load devices. The voltage across such devices tends to be large enough to be discernible using CMOS circuits making this approach useful to the implementation of CMOS/nano systems.

An illustration of a nanomemory with a load row can be seen in the left of Figure 5. From here it can be seen that to

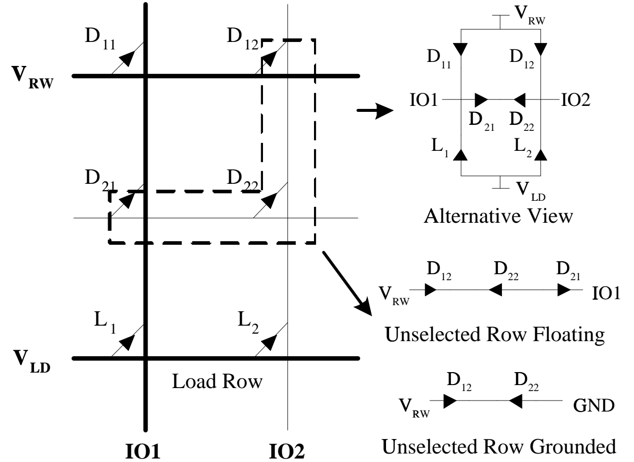

Figure 5: A 2×2 memory with load row (left) and the undesirable current path in this circuit (right).

	Floating		Grounded	
Mem. Size	worst '0'	worst '1'	worst '0'	worst '1'
2 × 2	442.4mV	1.188V	59.22mV	1.063V
4 × 4	915.2mV	1.006V	59.22mV	827mV
8 × 8	1.109V	787.4mV	59.22mV	596.3mV
16 × 16	1.119V	572.5mV	59.22mV	394.4mV
32 × 32	1.243V	390.9mV	59.22mV	239.2mV
64 × 64	1.265V	256.9mV	59.21mV	134.9mV

Table 1: Size limitations for memory where the unselected rows are left floating and the case where they are grounded. Grounding just the unselected rows allows for memory sizes up to at least 64×64.

read device D_{11}, a high voltage should be applied at V_{RW}. The voltage then read at node $IO1$ is the voltage across the load device L_1 which is in series with D_{11} between V_{RW} and V_{LO} (usually grounded for a read). Since these voltages are on an order of magnitude easily sensed by CMOS, this particular technique allows for easier access to a nanoscale memory.

Ideally, the output voltage only depends on the device being read (D_{11}) and its corresponding load device (L_1). This ideal case exists if parameter variations are negligible and all devices along the addressed row are programmed in the same state. If this is the case the voltages at each column are identical and no current flows through the undesirable circuit paths (middle right of Fig. 5). Of course, parameter variations are to be expected and it is unlikely that all bits along a row will be identical. This being the case, current will flow through unselected row devices in such a way that the output signals are degraded. In fact, the size of the array is still limited by the ratio between forward and reverse bias current just like it is when measuring a current at the output.

One way to reduce the size limitations of this nanoscale memory is to ground the unselected rows and columns (bottom right of Fig. 5). Given the structure of the memory array when using a load row, a reasonable design might include grounding the unselected rows while unselected columns remain floating. In fact, this is the common method used

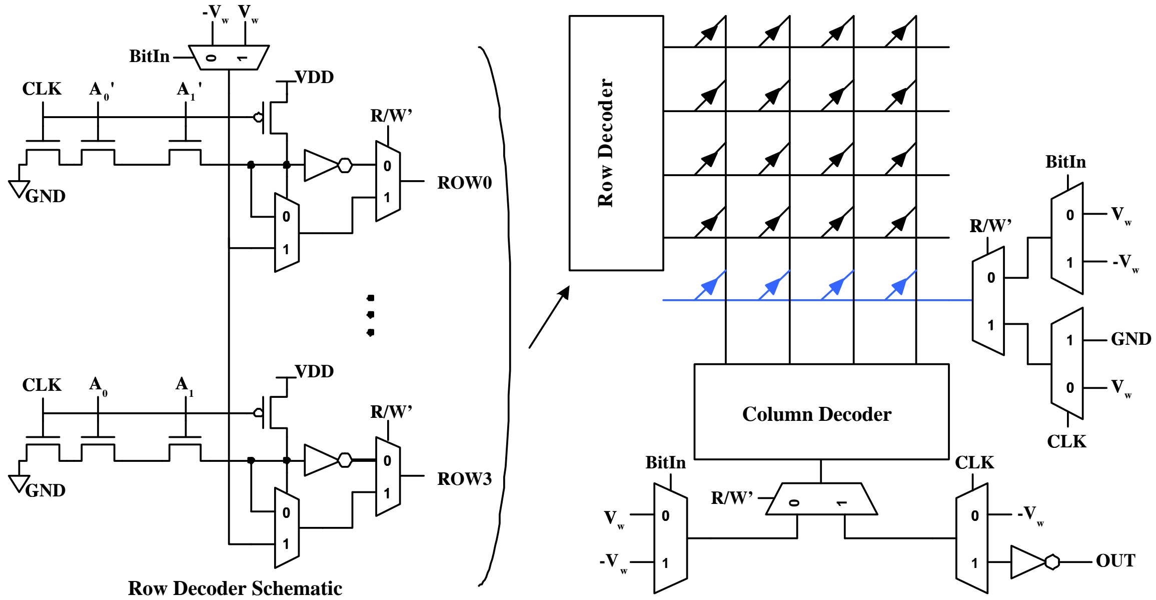

Figure 6: Illustration of proposed molecular memory architecture complete with required CMOS circuitry.

for the row decoders of an SRAM where each row in memory is driven by a driver pulling the row to either V_{DD} or GND [13]. Table 1 compares the size limitations for memory where the unselected rows are left floating with the case where they are grounded. Just as is the case when measuring current output, array size is significantly limited when the rows are floating. However, these results show that grounding just the unselected rows allows for memory sizes up to at least 64×64.

4.3 Methods for Reading and Writing

Designing an overall memory array using the load row technique also requires careful consideration of how the memory is to be written to and read from. In addition to the row and column decoders necessary for bit selection, the CMOS layer must also include circuitry for driving both selected and unselected (grounded) rows during a read, applying a large positive or large negative voltage during a write and selecting between read and write operations. These functions are most easily implemented using pass-gate or pass-transistor multiplexors but care must also be taken to ensure that the CMOS level circuitry doesn't become so dense as to negate any advantages from using nanoelectronics.

Fig. 6 shows how CMOS multiplexors could be used to read and write a molecular device series connected to a load. The two control signals are R/W' for selecting read or write and $BitIn$ for driving either a positive (write '1') or negative (write '0') voltage during a write operation. As illustrated, the load row is connected to either V_w or $-V_w$ during a write to ensure the load devices aren't written to.

For an array based circuit, the specific values of V_w and $-V_w$ must be carefully selected such that only the selected device is written to and no others are corrupted. The voltage V_w must be at least half the threshold for switching a single device to ensure a successful write. This leads to the following criteria for V_w:

$$\frac{1}{2} \cdot V_{toggle} \leq V_w < V_{toggle} \tag{1}$$

5. CMOS/NANO MEMORY SYSTEM DESIGN AND SIMULATION

The complete schematic for the molecular memory architecture proposed here including CMOS circuitry can be seen in Fig. 6. The CMOS column decoder for this memory could be a standard binary or k-hot decoder for selecting a single column. This selected column can then either drive the output or be driven by the appropriate voltage during a write. Similar to the multiplexor based circuitry for the column decoder I/O, the load row is driven with the appropriate voltage depending on whether or not the circuit is reading or writing.

The left side of Fig. 6 shows a more detailed schematic of the row decoder. This circuit is not very different than what might be used for an SRAM or DRAM with the exception that the write operation requires the $\pm V_w$ voltages. Which of these voltages are to drive the row during a write is determined using the multiplexor circuits shown. Also in the row decoder is the use of a clock signal (CLK) to ensure the row is driven with either V_{DD} (selected) or GND (unselected). The CLK signal appears in the NAND functions of the row decoder implemented using domino logic. The multiplexors for the column decoder and load row also use CLK to force the load devices to the high conductivity state every time CLK goes low during a read. This ensures the conductivity of each load device is known during a read without taking extra time for the operation.

Simulation results for the 4×4 molecular memory array based on the nitro device can be seen in Fig. 7. The simulation first writes to two memory locations: a '0' to '1111' on the top left corner and a '1' to '0000' on the bottom right. These locations were chosen to demonstrate that a write to one bit will not alter the state of other bits in the memory.

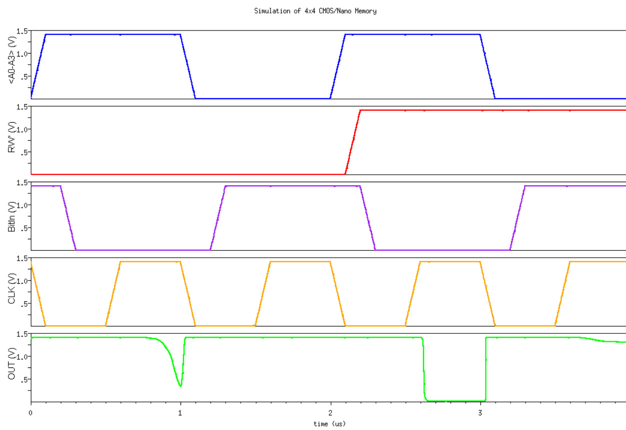

Figure 7: Simulation results for writing a zero and a one to different locations in a 4×4 nanomemory.

After the R/W' line goes high for a read operation it can be seen that the correct data has been stored to the two memory locations ('0' to '1111' and '1' to '0000').

6. CONCLUSION

This work has identified specific merits and potential issues when using molecular electronic devices in a hybrid CMOS/Nano memory circuit. Design solutions are described which address discussed limitations from both the device and circuit levels of abstraction. Specifically, from the circuits perspective, it has been shown that molecular devices can be used to load addressed memory such that the CMOS interface deals only with voltages and not currents. Such a design choice leads to CMOS circuitry that does not have to be as sensitive as would be required to sense the small currents (100pA) typical of molecular electronics.

This work shows that, from the perspective of circuit operation, integrating CMOS and nanoelectronic devices on the same die is feasible. Important to note, however, is that as the field of molecular electronics matures, device and circuit level properties and potential limitations (e.g., yields and parameter variations) will become more fully characterized. Future study will consist of including such characterizations in the simulation of memory circuits for accurately evaluating the effects of parasitics, noise, and parameter variations.

7. ACKNOWLEDGMENTS

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8. REFERENCES

[1] Y. Chen, G. Jung, D. A. A. Ohlberg, X. Li, D. R. Stewart, J. O. Jeppesen, K. A. Nielsen, J. F. Stoddart, and R. S. Williams. Nanoscale molecular-switch crossbar circuits. *Nanotechnology*, 14:462–468, 2000.

[2] C. P. Collier, G. Mattersteig, E. W. Wong, Y. Luo, K. Beverly, J. Sampaio, F. M. Raymo, J. F. Stoddart, and J. R. Heath. A [2]catenane-based solid state electronically reconfigurable switch. *Science*, 289:1172–1175, August 2000.

[3] Z. J. Donhauser, B. A. Mantooth, K. F. Kelly, L. A. Bumm, J. D. Monnell, J. J. Stapleton, D. W. Price, A. M. Rawlett, D. L. Allara, J. M. Tour, and P. S. Weiss. Conductance switching in single molecules through conformational changes. *Science*, 292(5525):2303–2307, June 2001.

[4] F.-R. F. Fan, J. Yang, L. Cai, D. W. Price, S. M. Dirk, D. V. Kosynkin, Y. Yao, A. M. Rawlett, J. M. Tour, and A. J. Bard. Charge transport through self-assembled monolayers of compounds of interest in molecular electronics. *J. Amer. Chem. Soc.*, 124(19):5550–5560, 2002.

[5] D. Goldhaber-Gordon, M. S. Montemerlo, J. C. Love, G. J. Opiteck, and J. C. Ellenbogen. Overview of nanoelectronic devices. *Proc. IEEE*, 85(4):521–540, April 1997.

[6] I. Kratochvilova, M. Kocirik, A. Zambova, J. Mbindyo, T. E. Mallouk, and T. S. Mayer. Room temperature negative differential resistance in molecular nanowires. *J. Mater. Chem.*, 12(10):2927–2930, 2002.

[7] J. G. Kushmerick, C. M. Whitaker, S. K. Pollack, T. L. Schull, and R. Shashidhar. Tuning current rectification across molecular junctions. *Nanotechnology*, 15(7):S489–S493, July 2004.

[8] P. A. Lewis, C. E. Inman, Y. Yao, J. M. Tour, J. E. Hutchinson, and P. S. Weiss. Mediating stochastic switching of single molecules using chemical functionality. *J. Amer. Chem. Soc.*, 126(39):12214–12215, 2004.

[9] C. Li, D. Zhang, X. Liu, S. Han, T. Tang, C. Zhou, W. Fan, J. Koehne, J. Han, M. Meyyappan, A. M. Rawlett, D. W. Price, and J. M. Tour. Fabrication approach for molecular memory arrays. *Appl. Phys. Lett.*, 82(4):645–647, January 2003.

[10] Y. Luo, C. P. Collier, J. O. Jeppesen, K. A. Nielson, E. Delonno, G. Ho, J. Perkins, H. Tseng, T. Yamamoto, J. F. Stoddart, and J. R. Heath. Two-dimensional molecular electronics circuits. *ChemPhysChem*, 3(6):519–525, June 2002.

[11] N. Majumdar, N. Gergel, D. Routenberg, J. C. Bean, L. R. Harriott, B. Li, L. Pu, Y. Yao, and J. M. Tour. Nanowell device for the electrical characterization of metal-molecule-metal junctions. *J. Vac. Sci. Technol. B*, 23(4):1417–1421, July 2005.

[12] N. Majumdar et al. *Journal of Electronic Materials*. accepted September 2005.

[13] J. M. Rabaey, A. Chandrakasan, and B. Nikolić. *Digital Integrated Circuits: A Design Perspective*. Prentice Hall, second edition, 2003.

[14] M. A. Reed. Molecular-scale electronics. *Proc. IEEE*, 87(4):652–658, April 1999.

[15] M. A. Reed, J. Chen, A. M. Rawlett, D. W. Price, and J. M. Tour. Molecular random access memory cell. *Appl. Phys. Lett.*, 78(23):3735–3737, June 2001.

[16] G. S. Rose, M. M. Ziegler, and M. R. Stan. Large-signal two-terminal device model for nanoelectronic circuit analysis. *IEEE Trans. VLSI Syst.*, 12(11):1201–1208, November 2004.

[17] C. Zhou, M. R. Deshpande, M. A. Reed, L. Jones II, and J. M. Tour. Nanoscale metal/self-assembled monolayer/metal heterostructures. *Appl. Phys. Lett.*, 71(5):611, November 1997.

[18] M. M. Ziegler and M. R. Stan. Design and analysis of crossbar circuits for molecular nanoelectronics. In *Proceedings IEEE Conference on Nanotechnology*, pages 323–327, August 2002.